EE 3060: Special Projects

Research and Development of a Radiofrequency Amplifier

Darren Moran

89-555-0086

Instructor: Mr John Scalzo

Abstract

This report outlines a research project in designing a radiofrequency amplifier. The report looks at the research into the different stages of the design process, before overlooking the implementation of these design methods and the analysis of the final system.

Contents

Introduction

The field of radiofrequency (RF) technologies covers many different devices which operate using signals of large frequencies. The purpose of an RF amplifier is to increase the gain of an RF signal at a specified operating frequency. An RF amplifier circuit can be designed so as to take a high frequency signal as the input, producing an increased gain signal at the output. A transistor can be used as the basis of the amplifier circuit, but where low frequency amplifier circuits could consist solely of passive components, an RF amplifier should consider transmission line theory and other high frequency techniques to diminish error in the operation of the circuit.

The aim of this project was to undertake research into the operations of RF amplifiers and the techniques that can be implemented in the design of such a system, before using these techniques along with various software tools to design and manufacture an operational RF amplifier.

The transistor chosen for the basis of the design was the BFG403W NPN wideband transistor of NXP Semiconductors. The targeted operational frequency was 1GHz with a desired gain of greater than 10 dB.

Background Theory

1. Transistor Biasing

The first stage of the design process for an RF amplifier is to bias the transistor. A bias circuit is required to provide the desired amount of voltage and current at each specific part of the transistor. The voltage and current values can be found using the S-parameters of the transistor, which are provided from the transistor manufacturer. These parameters are measured at specific voltage and current values, and across a frequency range, which are subsequently essential for all further stages of the amplifier circuit design process.

An example transistor biasing circuit is shown in figure 1.

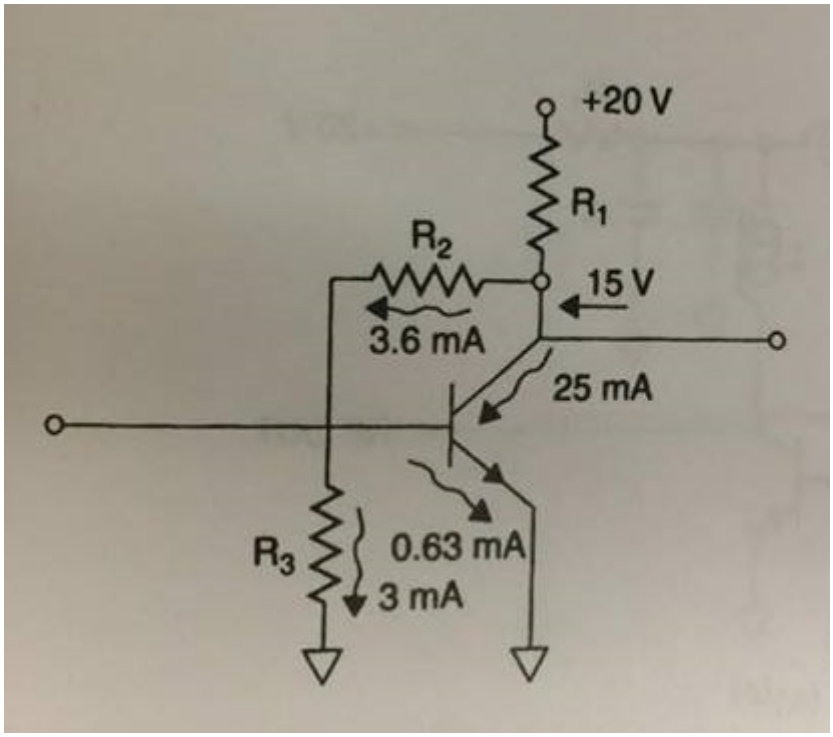

Figure 1. Example Transistor Bias Circuit

In this circuit it is clear to see that the resistors are enabling the different sections of the transistor to receive the appropriate current and voltage values necessary for correct operation. The values of resistor can be calculated by using the information provided by the transistor manufacture for the S-parameters. The two main pieces of information an S-parameter file provides for the biasing circuit is the collector voltage and current, as well as the DC current gain β. The base current is required to be the collector current value divided by the current gain, with the shunt path carrying roughly 5 times as much. This can be seen in the example, where the base current is 0.63mA, with the current through R3 roughly 5 times this at 3mA. The turn on voltage for the transistor is 0.75V and hence the resistance of R3 can be calculated using:

$$R3 = \frac{Base\ Voltage}{5\ Base\ Current} \quad (1)$$

The value of R2 can subsequently be calculated using:

$$R2 = \frac{Collecter\ Voltage - Base\ Voltage}{6\ Base\ Current} \quad (2)$$

Finally R1 can be calculated using:

$$R1 = \frac{Supply\ Voltage - Collector\ Voltage}{Collector\ Current + R2\ Current} \quad (3)$$

By implementing these resistor values into a bias circuit it is possible to power the transistor. However, before this can be done, considerations must be made for the RF signal passing through the circuit. Due to the high nature of the frequency signals present in the circuit, the resistors could fail to perform as expected due to parasitic changes, and therefore it is necessary to utilise a high frequency blocking section to the bias circuit. This can be achieved using either discrete components or distributed, as shown in figures 2 and 3.

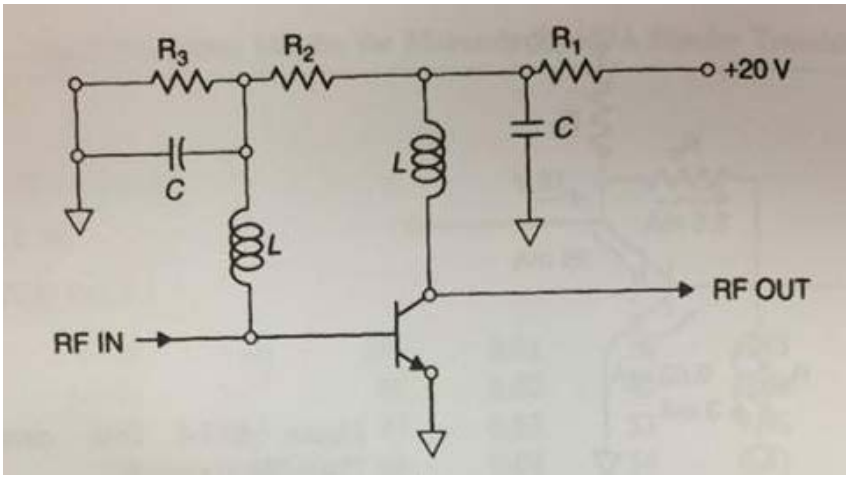

Figure 2. Transistor Biasing Circuit with Discrete Components

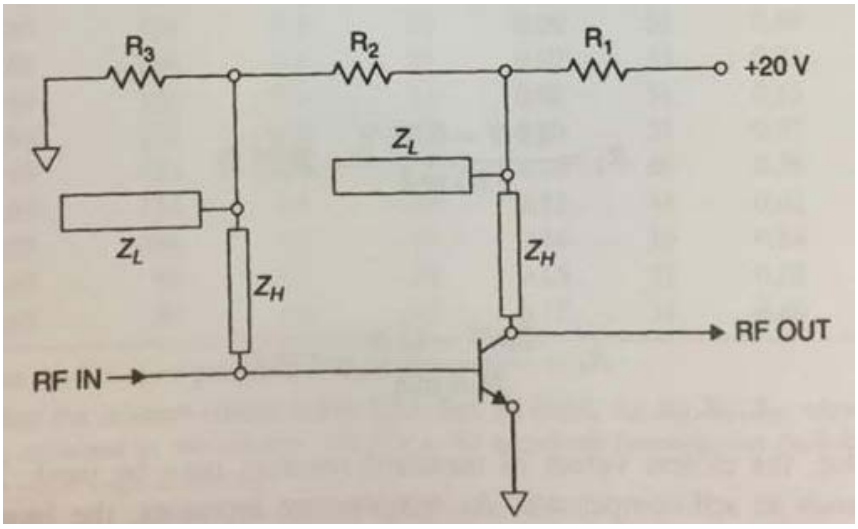

Figure 3. Transistor Biasing Circuit with Distributed Components

For the distributed method the discrete capacitors and inductors are replaced by quarter wavelength transmission lines, short circuit for the inductors and open circuit for the capacitors. The characteristic impedance of the inductive lines is to be very high, with the capacitive lines very low, so as to effectively block RF signals from entering the bias circuit.

At this stage all parameters can be calculated to create an operational bias circuit for a transistor at a desired frequency.

2. Amplifier Stability

The next consideration in amplifier design is the stability of the system. Under certain conditions it is possible that an amplifier may apply gain to unwanted reflected signals and cause oscillation. To prevent this, there are different stability techniques which can be applied. An excellent graphical tool which can be used to stabilise an amplifier design is the stability circles method. This works by mapping a circle for both the output stability and input stability, with each circle created using the S-parameters and input and output reflection coefficients. These circles can be plotted along with a smith chart centred at the origin, with any overlapping regions representing impedances that would produce instability. An example of stability circles is shown in figure 4.

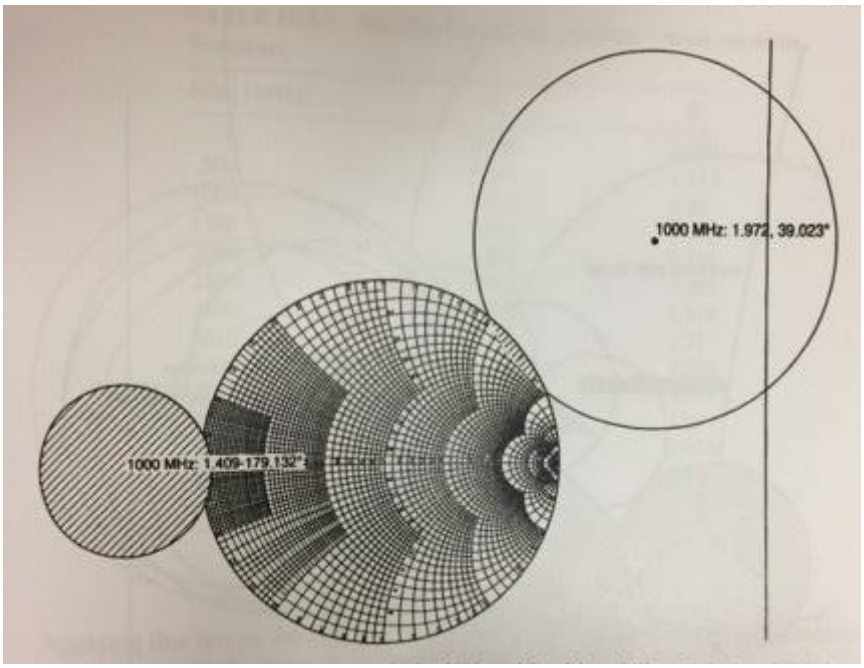

Figure 4. Example of input and output stability circles

To obtain the centre point and radius of the stability circles requires the use of empirical formulae. The main component of these equations are the S-parameters for the transistor at the desired operational frequency. The following equations can be used to obtain the centre and radius values for both the input and output stability circles:

$$\Delta = S11 * S22 - S12 * S21 \quad (4)$$

$$CL = \frac{S22^* - \Delta^* S11}{|S22|^2 - |\Delta|^2} \quad (5)$$

$$RL = \left| \frac{S12 * S21}{|S22|^2 - |\Delta|^2} \right| \quad (6)$$

$$CS = \frac{S11^* - \Delta^* S22}{|S11|^2 - |\Delta|^2} \quad (7)$$

$$RS = \left| \frac{S12 * S21}{|S11|^2 - |\Delta|^2} \right| \quad (8)$$

To stabilise the system, components can be added at the source and load of the transistor so as to move the stability circles away from the smith chart, eradicating the overlapping regions.

3. Unilateral Gain

To simplify the design of an RF amplifier system, the unilateral assumption can be made so as to ignore the feedback S-parameter S12. To do this, S12 is assumed to be 0, and this modification enables simplified calculations to be performed for the gain of the system at the expense of some gain uncertainty. By setting S12 to 0 the transducer gain equation becomes:

$$Gtu = Gs * G0 * GL \quad (9)$$

Where:

$$Gs = \frac{1 - |\Gamma s|^2}{|1 - S11\Gamma s|^2} \quad (10)$$

$$G0 = |S21|^2 \quad (11)$$

$$GL = \frac{1 - |\Gamma L|^2}{|1 - S22\Gamma L|^2} \quad (12)$$

The maximum source and load gains can be obtained by setting the reflection coefficient equal to the conjugate of the relevant S-parameter - i.e. Γs = $S11^*$ and ΓL = $S22^*$. In order to obtain these values from the circuit, the source and load impedances must be transformed to be Zin^* and $Zout^*$ respectively, where:

$$Zin = \frac{1 + S11}{1 - S11} \quad (13)$$

$$Zout = \frac{1 + S22}{1 - S22} \quad (14)$$

On transforming the 50 ohm source and load impedances to the respective conjugate impedances, the transducer gain would be maximised under the unilateral assumption.

Due to this assumption, there is some uncertainty in the final gain obtained using the unilateral design, which can be calculated using the unilateral figure of merit or U.

$$U = \frac{|S11||S21||S12||S22|}{(1-|S11|^2)(1-|S22|^2)} \quad (15)$$

This value can be used to find the uncertainty upper bounds and lower bounds. The upper bound is found using:

$$\frac{1}{(1-U)^2} \quad (16)$$

The lower bound is found using:

$$\frac{1}{(1+U)^2} \quad (17)$$

The calculated values from these equations can be converted to decibels to obtain a maximum and minimum boundary for the overall gain of the system.

4. Gain Circles

When designing an RF amplifier circuit it may not always be ideal to have matching networks to a specific complex load, and hence a useful simplification technique is the use of gain circles. Gain circles can be drawn on a smith chart surrounding the point of maximum gain, with each circle representing a sacrifice of 1dB working away from the maximum point. This can be particularly useful when it is preferred to only deal with resistive loads, and hence the load can be chosen from the point one of the gain circles crosses the real line on the smith chart.

In a similar style to the stability circles, the gain circle parameters are calculated using the S-parameters, with use of the maximum source and load gains calculated using equations 10 and 12. The following equations are used for the input gain circles:

$$gs = Gs * \frac{1}{1-|S11|^2} \quad (18)$$

$$Cgs = \frac{gs*S11^*}{1-|S11|^2(1-gs)} \quad (19)$$

$$rgs = \frac{\sqrt{1-gs}(1-|S11|^2)}{1-|S11|^2(1-gs)} \quad (20)$$

Where Gs is the maximum source gain found in equation 10, with 1dB removed for each circle parameters desired.

An example of input gain circles surrounding the maximum input impedance point is shown in figure 5.

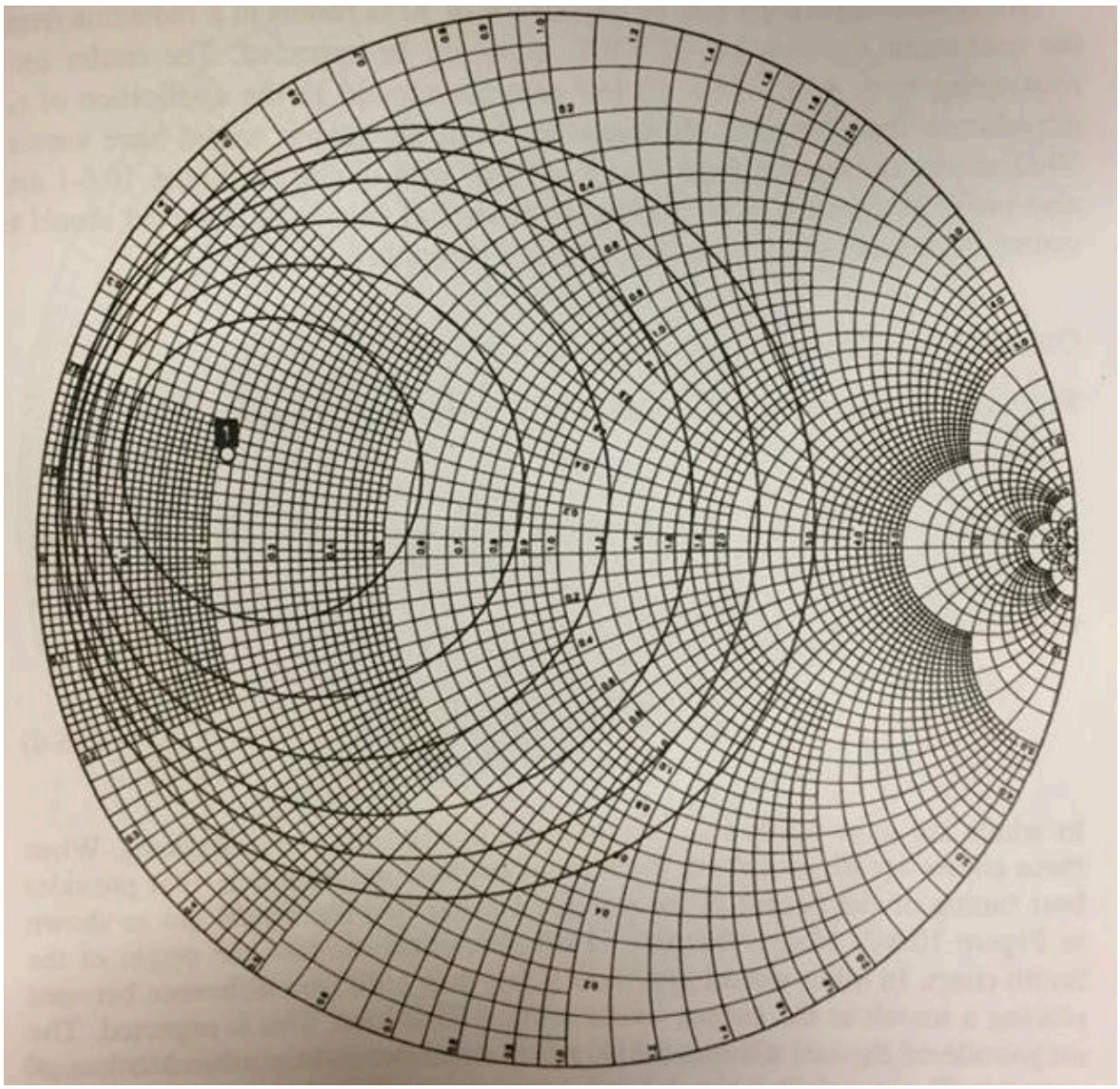

Figure 5. Example of input gain circles surrounding the maximum gain source point

Each circle represents a decrease in gain of 1dB.

The following equations are used for the output gain circles:

$$gL = GL * \frac{1}{1-|S22|^2} \tag{21}$$

$$CgL = \frac{gL*S22^*}{1-|S22|^2(1-gL)} \tag{22}$$

$$rgL = \frac{\sqrt{1-gL}(1-|S22|^2)}{1-|S22|^2(1-gL)} \tag{23}$$

Where GL is the maximum load gain found in equation 12, with 1dB removed for each circle parameters desired.

An example of output gain circles surrounding the maximum output impedance point is shown in figure 6.

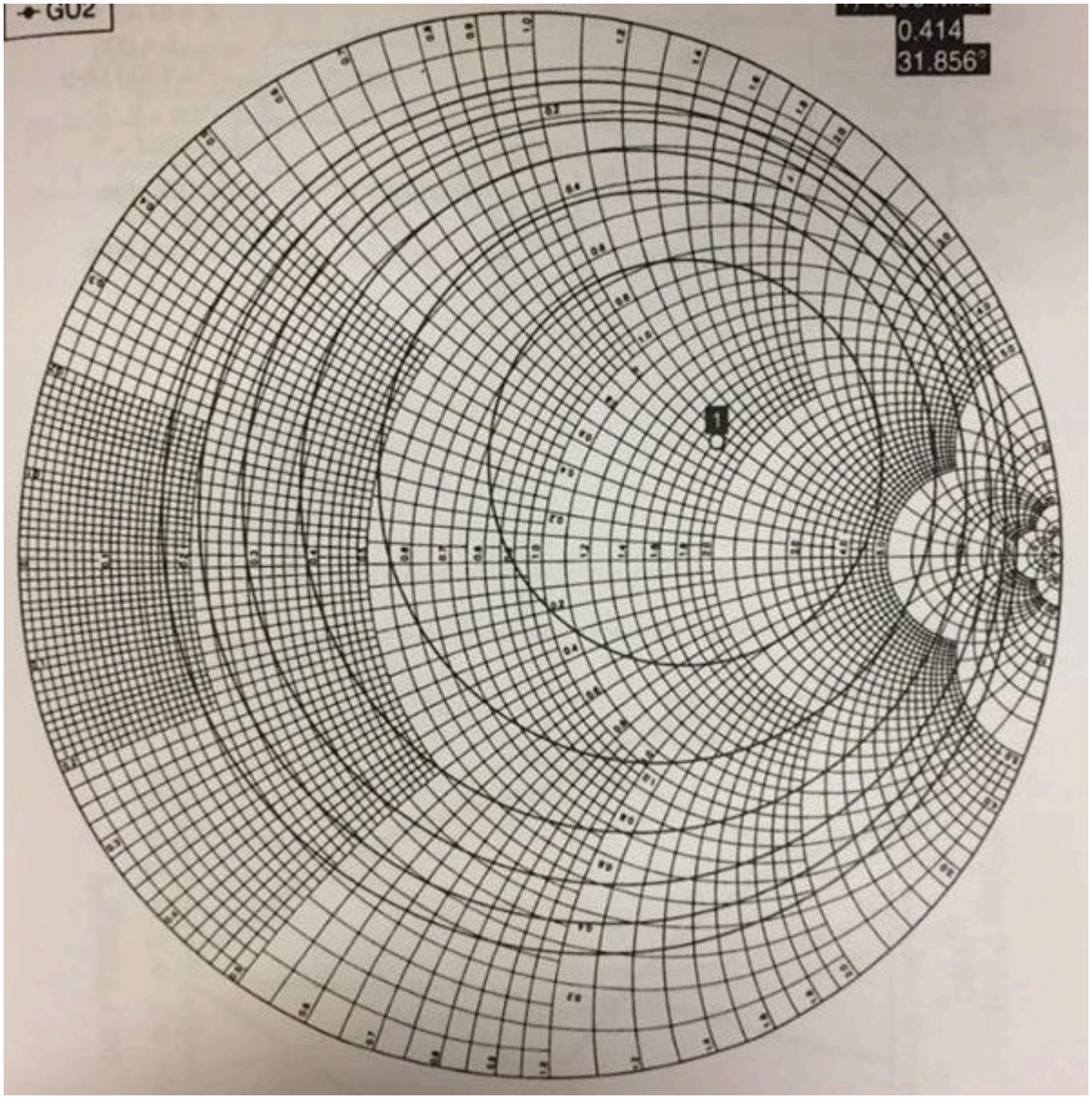

Figure 6. Example output gain circles surrounding the maximum gain load point

It is possible to design the input and output matching networks of an RF amplifier circuit so as to transform 50 ohms to a point on the real line which is crossed by one of the gain circles. By using these points it is known that the maximum possible gain will be the number of decibels subtracted from the total maximum gain.

5. Bilateral Design

For the maximum results in an RF amplifier design the bilateral method must be used which takes the feedback S-parameter S12 of the transistor into consideration. This involves generating new equations for the source and load reflection coefficients, which effectively collate all the necessary parameters to produce a value that can be used to obtain the maximum source and load impedances. The equation for the source reflection coefficient is:

$$\Gamma SM = C1^* \left[\frac{B1 \pm \sqrt{B1^2 - 4|C1|^2}}{2|C1|^2}\right] \quad (24)$$

Where:

$$C1 = S11 - \Delta S22^* \quad (25)$$

$$B1 = 1 + |S11|^2 - |S22|^2 - |\Delta|^2 \quad (26)$$

The equation for the load reflection coefficient is:

$$\Gamma LM = C2^* \left[\frac{B2 \pm \sqrt{B2^2 - 4|C2|^2}}{2|C2|^2}\right] \quad (27)$$

Where:

$$C2 = S22 - \Delta S11^* \quad (28)$$

$$B2 = 1 - |S11|^2 + |S22|^2 - |\Delta|^2 \quad (29)$$

These values can then be used to obtain the corresponding source and load impedances that would produce maximum gain. This maximum bilateral gain value can be found using equation 30.

$$Gt = \frac{(1-|\Gamma SM|^2)|S21|^2(1-|\Gamma LM|^2)}{|(1-S11*\Gamma SM)(1-S22*\Gamma LM)-S12*S21*\Gamma SM*\Gamma LM|^2} \quad (30)$$

When designing an RF amplifier the choice can be made between the different options, with the bilateral method producing the most accurate results. The simplified unilateral design method can be chosen as an alternative at the expense of efficiency in the final system.

Design

1. Transistor Biasing

The first stage of the design process was to select a transistor for which the circuit would be based around. The transistor chosen was the BFG403W from NXP semiconductors, with the aim of amplification at operational frequency of 1 GHz. The S-parameter information for the transistor is shown in figure 7.

```
! Filename: 23bfg403.001
! BFG403W Field A1
! V1=8.791E-001V,V2=2.000E+000V, I1=4.308E-005A, I2=3.000E-003A
# GHz   S   MA   R 50
!                S11              S21              S12              S22
!Freq(GHz)  Mag     Ang      Mag     Ang      Mag     Ang      Mag     Ang
   0.040    0.879  -1.364    7.211 177.009    0.001  31.643    0.991  -0.662
   0.100    0.883  -3.156    7.093 175.130    0.001  92.445    0.992  -2.015
   0.200    0.880  -6.244    7.069 170.888    0.003  84.816    0.991  -4.220
   0.300    0.875  -9.327    7.029 167.027    0.004  82.310    0.989  -6.350
   0.400    0.867 -12.180    6.996 162.549    0.005  80.116    0.985  -8.501
   0.500    0.856 -15.613    6.947 158.123    0.007  77.686    0.980 -10.569
   0.600    0.845 -18.511    6.847 153.997    0.008  75.120    0.975 -12.617
   0.700    0.832 -21.347    6.737 150.043    0.009  73.410    0.969 -14.670
   0.800    0.819 -24.306    6.645 146.020    0.010  71.465    0.962 -16.669
   0.900    0.804 -27.038    6.546 142.123    0.011  69.706    0.955 -18.648
   1.000    0.787 -29.852    6.441 138.225    0.012  67.938    0.947 -20.577
   1.100    0.771 -32.477    6.324 134.513    0.013  66.236    0.939 -22.379
   1.200    0.754 -35.069    6.204 130.774    0.014  64.926    0.931 -24.257
   1.300    0.736 -37.591    6.074 127.188    0.015  63.344    0.923 -26.078
   1.400    0.718 -39.992    5.959 123.705    0.016  61.999    0.914 -27.815
   1.500    0.698 -42.441    5.834 120.220    0.017  60.724    0.905 -29.520
```

Figure 7. Table of S-Parameters for the BFG403W

The S-parameter data was obtained with a collector voltage of 2 V and current of 3 mA, whilst the DC current gain of the transistor, β, was 80. These values enabled the calculation of the bias circuit resistor values R1, R2 and R3 using equations 1, 2 and 3. R1 was calculated as follows:

$$R1 = \frac{Supply\ Voltage - Collector\ Voltage}{Collector\ Current + R2\ Current}$$

$$R1 = \frac{6 - 2}{3mA + 0.225mA}$$

$$\boldsymbol{R1 = 1.24\ k\Omega}$$

R2 was calculated as follows:

$$R2 = \frac{Collecter\ Voltage - Base\ Voltage}{6\ Base\ Current}$$

$$R2 = \frac{2 - 0.75}{0.225mA}$$

$$\boldsymbol{R2 = 5.56k\Omega}$$

R3 was calculated as follows:

$$R3 = \frac{Base\ Voltage}{5\ Base\ Current}$$

$$R3 = \frac{0.75}{0.1875mA}$$

$$\boldsymbol{R3 = 4k\Omega}$$

These values were then used to create a model of the bias circuit on the simulation software Multisim, with the completed circuit model shown in figure 8.

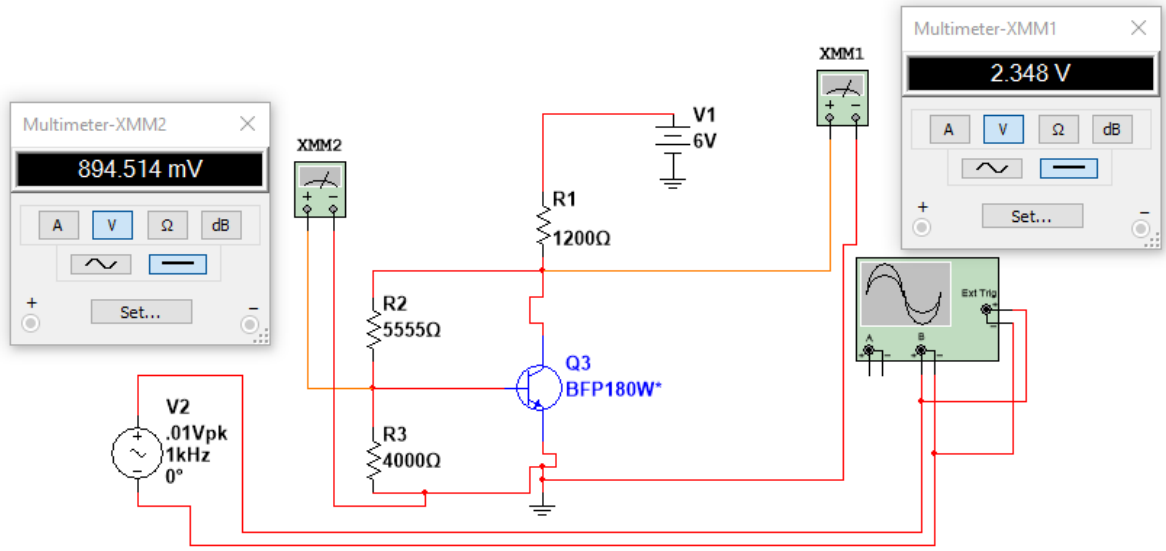

Figure 8. Bias circuit simulation on Multisim

The simulation showed that these resistor values combined with a 6V DC supply would successfully deliver the required values of current and voltage to ensure the transistor was operational, with a base voltage reading of 0.89 V and collector voltage reading of 2.35 V.

The next stage of the bias circuit was to design the distributed elements to block the RF signals. These were to be two inductive quarter wavelength transmission lines and two capacitive quarter wavelength transmission lines. For the inductive elements, the characteristic impedance was to be 150 Ω, with the capacitive elements having a characteristic impedance of 25 Ω. By using empirical formulae for transmission line theory, the characteristics of these lines were calculated. The transmission line characteristics are shown in table 1.

Table 1. Calculated transmission line parameters using empirical formulae

Desired Z0(Ω)	Calculated Z0(Ω)	Width(mils)	εeff	Length(mils)
25	25.396	300	3.776	1516
150	151.26	6	3.022	1703

To confirm the accuracy of these calculations, Sonnet simulation software was used to model and simulate the transmission lines. The sonnet model for the 25 ohm line is shown in figure 9.

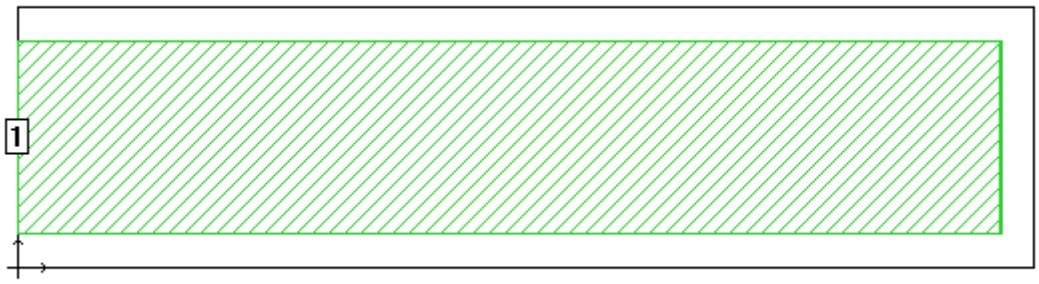

Figure 9. Sonnet model of 25 ohm transmission line

This model was then simulated at 1 GHz with the values for characteristic impedance and effective dielectric constant compared with those from the empirical formulae.

```
Frequency:  0.996 GHZ
  Frequency completed Tue Apr 25 03:52:39 2017.
  De-embedded S-Parameters. 50.0 Ohm Port Terminations.
  Magnitude/Angle. Touchstone Format.
    0.99600000 0.985524 -177.4
    !< P1 F=0.996 Eeff=(3.42699959 -0.0706068) Z0=(22.8687317 0.17910728) R=2.93164833 C=0.84405823

Frequency:  1.058 GHZ
  Frequency completed Tue Apr 25 03:52:45 2017.
  De-embedded S-Parameters. 50.0 Ohm Port Terminations.
  Magnitude/Angle. Touchstone Format.
    1.05800000 0.985387 177.69
    !< P1 F=1.058 Eeff=(3.42747776 -0.0703991) Z0=(22.8642466 0.17999571) R=2.75906066 C=0.84386996
```

Figure 10. Simulation results for 25 ohm transmission line in Sonnet

From the simulation of the calculated transmission line parameters it can be seen that the characteristic impedance is 22.8 ohms which is ≈25 ohms, the desired characteristic impedance.

At this stage the 150 ohm line was modelled on sonnet. The sonnet model for the 150 ohm line is shown in figure 11.

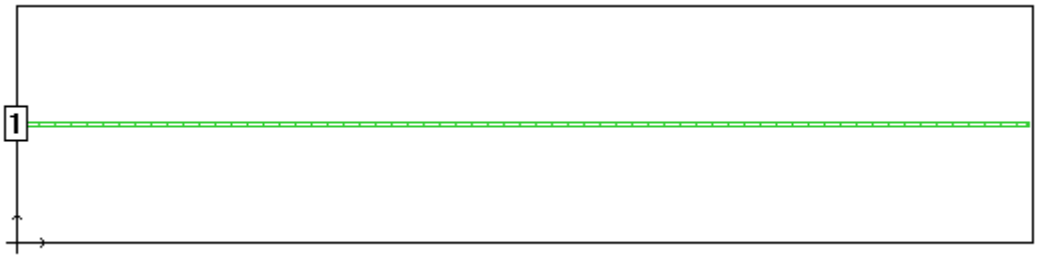

Figure 11. Sonnet model for the 150 ohm transmission line

This model was then simulated to observe the characteristic values at 1 GHz. The simulation results are shown in figure 12.

```
Frequency:  1.004 GHZ
  Frequency completed Tue Apr 25 03:55:24 2017.
  De-embedded S-Parameters. 50.0 Ohm Port Terminations.
  Magnitude/Angle. Touchstone Format.
    1.00400000 0.860984 170.81
    !< P1 F=1.004 Eeff=(3.03046771 -0.0941452) Z0=(151.989775 0.21629193) R=86.572745 C=0.02733593
```

Figure 12. Sonnet simulation results for 150 ohm transmission line

From these results it can be seen that the simulated characteristic impedance is 151.9 ohms which is ≈150 ohms, the desired characteristic impedance. Both the calculated and simulated values are shown in table 2.

Table 2. Calculated values and simulated values using Sonnet

Equation/Sonnet	**Desired Z0(Ω)**	**Calculated Z0(Ω)**	**Width(mils)**	**εeff**	**Length(mils)**
Equation	25	25.396	300	3.776	1516
Sonnet	25	22.868	300	3.427	1516
Equation	150	151.26	6	3.022	1703
Sonnet	150	151.99	6	3.03	1703

The simulation results proved that the calculations were accurate and that the values determined could be implemented in the manufacture of the circuit. At this stage all parameters for the bias circuit had been calculated and were ready to be used in the final system design.

2. Amplifier Stability

The next stage of the amplifier design was to use Matlab software to compute the different stability parameters of the transistor. Firstly the S-parameters were entered, and subsequently used to calculate the input and output reflection coefficients. The input and output stability circle parameters were then calculated using equations 5, 6, 7 and 8. By plotting the cirlces along with a smith chart centred at the origin, it was possible to determine the stability of the circuit. The stability circles are shown in figure 13.

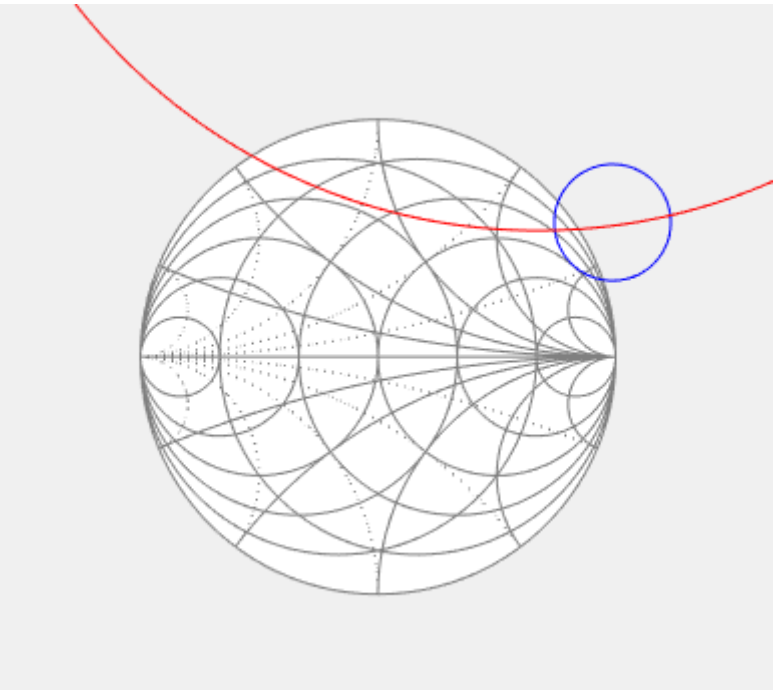

Figure 13. Initial Input and Output Stability Circles

The input stability circle is depicted in red with the output stability circle depicted in blue. From this graph it can be seen that there are areas of instability at both the input and the output of the transistor. Although the circuit will be matched to a 50 ohm source and load, it is best to ensure that at the operational frequency of 1 GHz the circuit will be stable for any load and source impedance value. Therefore, to stabilise the system, a shunt resistor of 100 ohms was added at the output of the circuit. By using ABCD transformations, a new set of S-parameters were calculated with the shunt resistor factored in. The stability of this system could be tested using the same matlab routine.

The results for the updated stability circles are shown in figure 14.

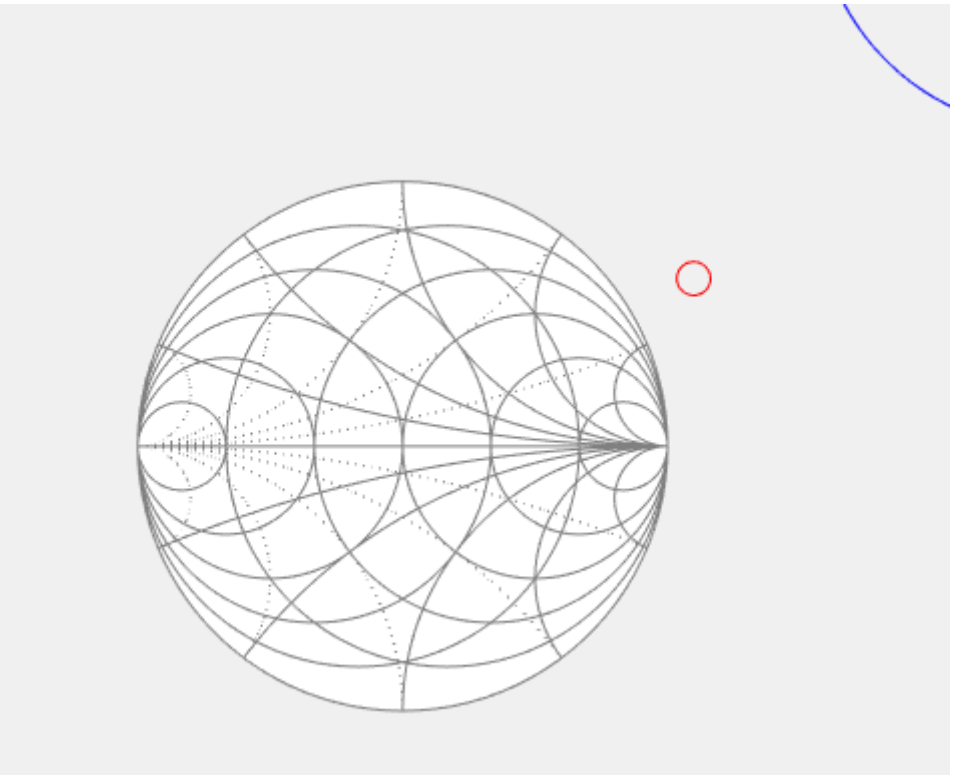

Figure 14. Stability circles for new system

From this graph it can be seen that despite only altering the impedance at the output, both the input and output stability circles have moved outside of the smith chart, and hence the system is now stable for all source and load impedance values at 1 GHz.

3. Gain Calculations

To simplify the design the unilateral method was chosen, with the aim of using gain circles to find purely resistive source and load impedances that could be used to obtain an adequate level of system gain. The first stage of the unilateral design process was to determine the maximum gain that would be available from perfect matching, with the unilateral figure of merit used to find the uncertainty in this value of gain. Using equation 9 at maximum gain conditions, the maximum gain was found to be:

$$Gtu = Gs * G0 * GL$$

$$Gtu = 57.0169$$

$$\boldsymbol{Gtu = 17.56\ dB}$$

Using equations 15, 16 and 17, the uncertainty was found to be ± 1 dB. This meant that at the maximum matched impedances the system would produce a gain of 17.56 ± 1 dB.

At this stage the source and load gain circles could be observed to see if it would be possible to sacrifice some gain in order to have purely resistive source and load impedances. The input gain circle parameters were determined using equations 18, 19 and 20, with circles plotted for losses of 1 dB, 2 dB and 3 dB. The input gain circles are shown in figure 15.

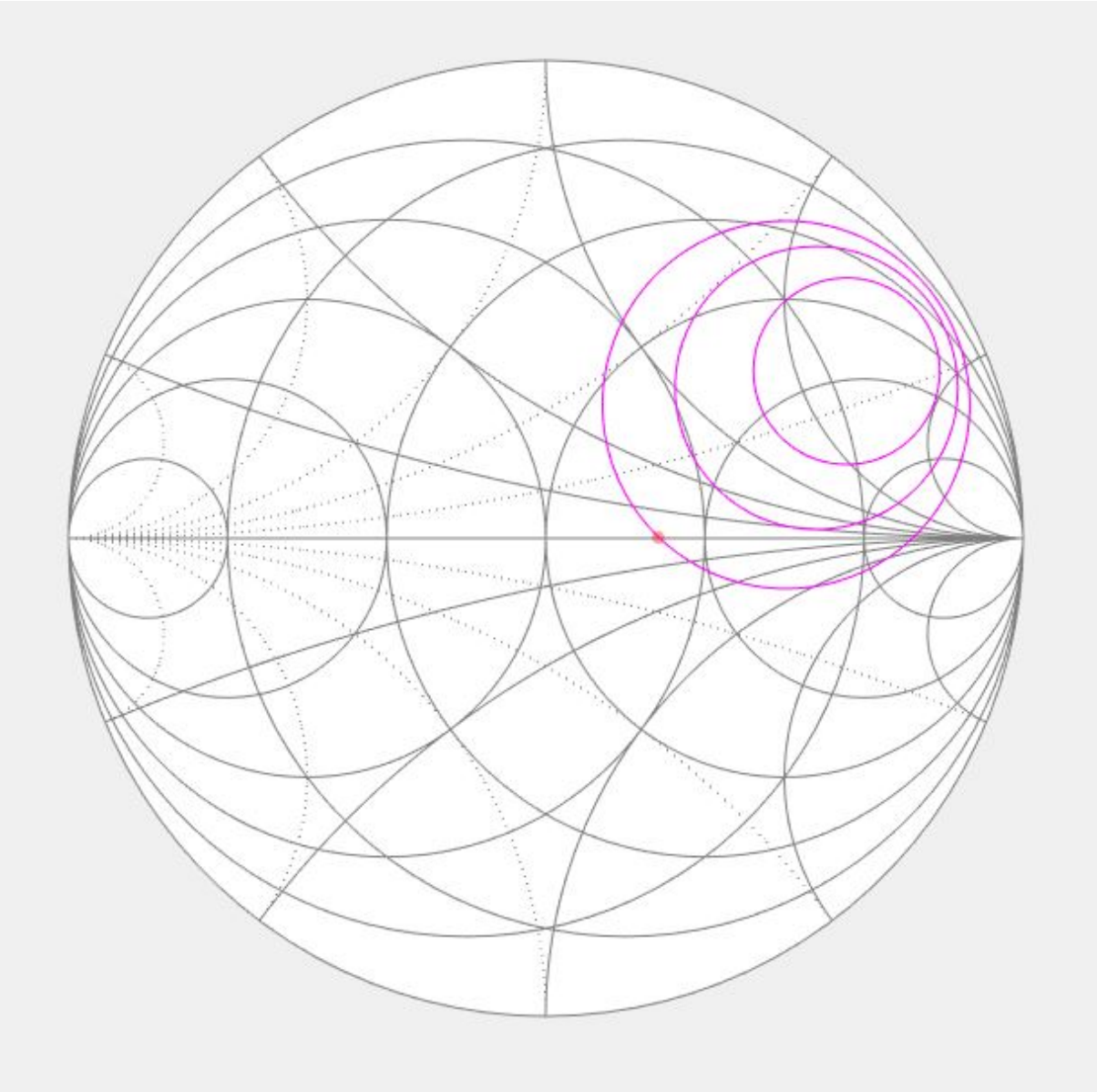

Figure 15. Input gain circles

From this graph it can be seen that in order to use a purely resistive source impedance, 3dB of gain must be sacrificed. The desired resistive impedance value can be found at the point where the 3 dB gain circle crosses the real axis. From this procedure it is found that the source of the system is desired to be 82 Ω.

The output gain circle parameters were then calculated using equations 21, 22 and 23, with a circle plotted for 1 dB gain loss. The output gain circle is shown in figure 16.

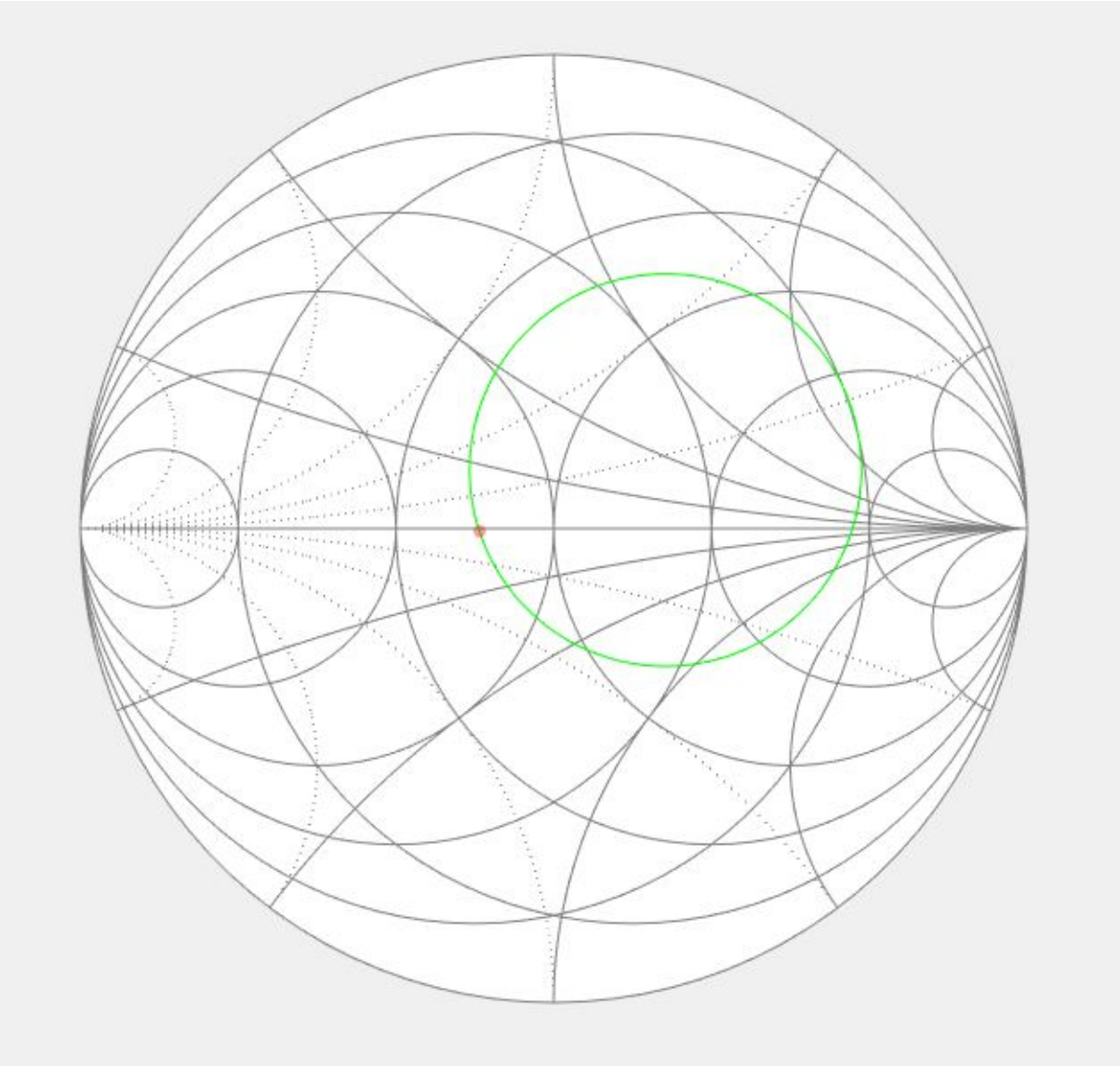

Figure 16. Output gain circles

From this graph it can be seen that in order to use a purely resistive load impedance, 1dB of gain must be sacrificed. The desired resistive impedance value can be found at the point where the 1 dB gain circle crosses the real axis. From this procedure it is found that the load of the system is desired to be 36 Ω.

By using the unilateral design method with the source and load matched to 82 and 36 ohms respectively, the maximum total gain of the system is calculated to be 13.56 ± 1 dB.

4. Matching Network Design

With the desired source and load impedance values for the system calculated, the next step was to design a matching network at both the input and output of the system to transform 50 Ω to the desired values of 82 Ω and 36 Ω. To begin the input matching network design, both points were drawn on a smith chart to show the quarter wavelength transformation that was to take place. The smith chart with the input quarter wavelength transformation from 50 ohms to 82 ohms is shown in figure 17.

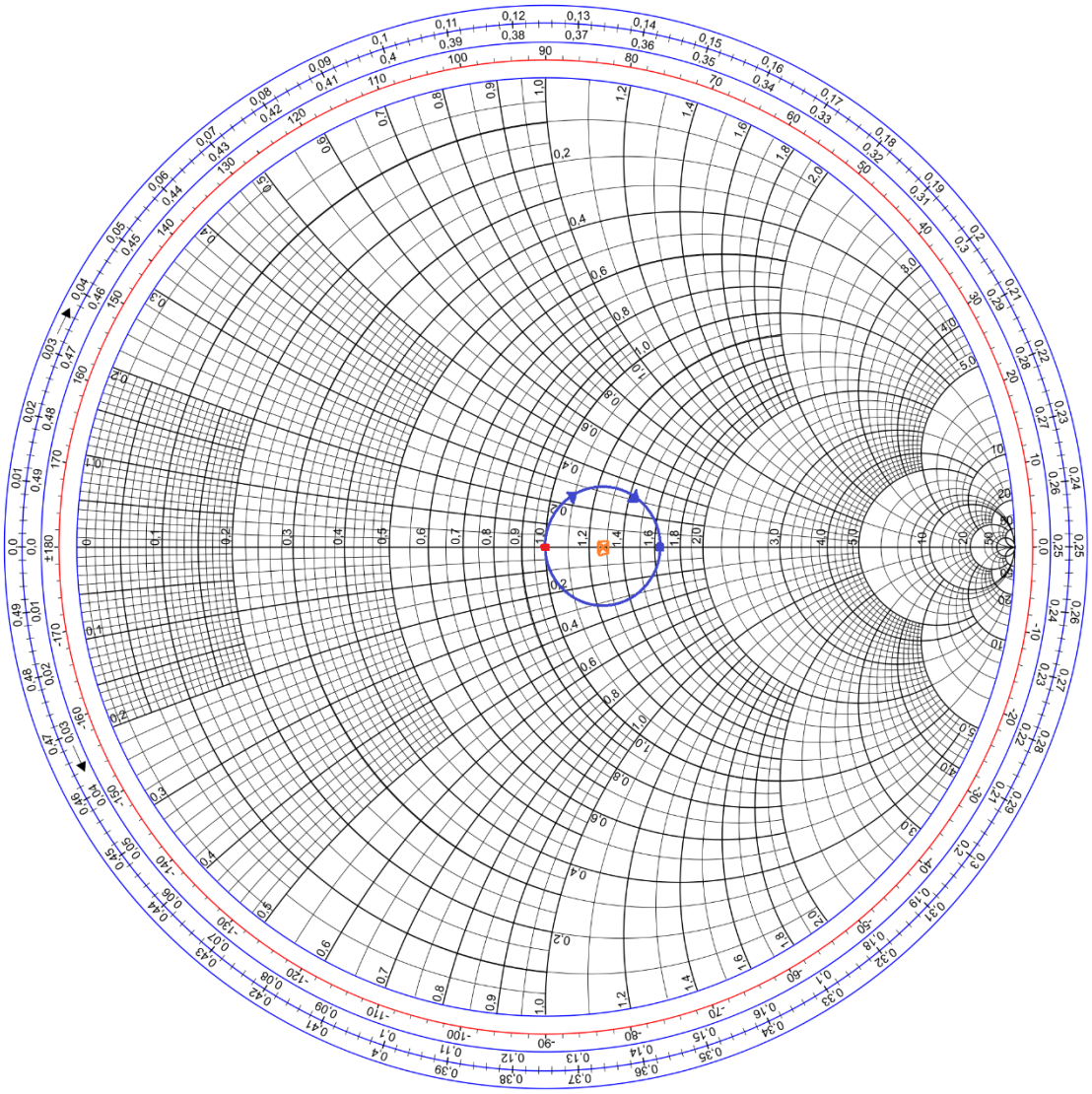

Figure 17. Smith chart with quarter wavelength transformation at source of the system

From transmission line theory it is known that the centre point of a quarter wavelength transformation circle is the characteristic impedance of the quarter wavelength transmission line. The smith chart shows that this centre point is at an impedance of 64 Ω and hence a transmission line of characteristic impedance 64 ohms and length λ/4 is required to transform 50 ohms to the required source impedance of 82 Ω.

By using empirical formulae from transmission line theory, the characteristics of this line were calculated. The transmission line characteristics are shown in table 3.

Table 3. Calculated characteristics using empirical formulae

Desired Z0(Ω)	Calculated Z0(Ω)	Width(mils)	εeff	Length(mils)
64	63.585	72	3.343	1614

As with the transmission lines in the bias circuit, sonnet software was used to simulate the transmission line to determine the accuracy of the calculations and ensure the dimensions calculated would be fit for use in the final design. The sonnet model for the 64 ohm quarter wavelength transformer is shown in figure 18.

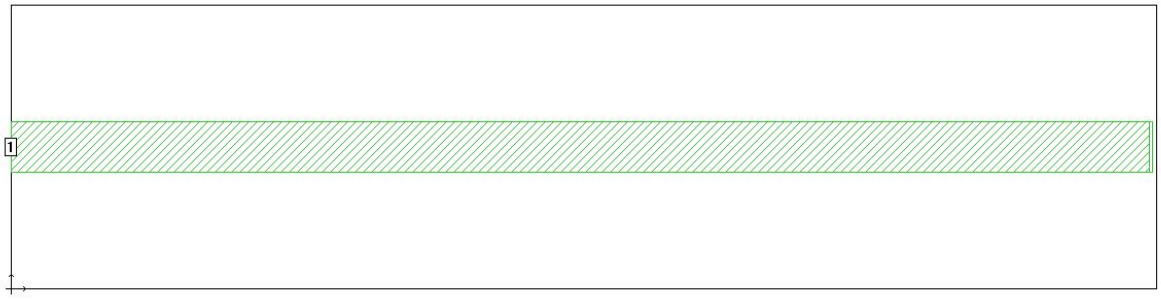

Figure 18. Sonnet model of 64 ohm transmission line

The results from simulating this model at 1 GHz are shown in figure 19.

```
Frequency:  1.004 GHZ
  Frequency completed Wed Apr 26 01:55:06 2017.
  De-embedded S-Parameters. 50.0 Ohm Port Terminations.
  Magnitude/Angle. Touchstone Format.
    1.00400000 0.959276 177.04
    !< P1 F=1.004 Eeff=(3.25169782 -0.0693192) Z0=(62.3427397 0.43476361) R=11.5800447 C=0.21093906
```

Figure 19. Sonnet Simulation results for 64 ohm transmission line

From the simulation it can be seen that the calculated measurements will produce a sufficient characteristic impedance to transform correctly, with the calculated value of 63.585 ohms being roughly the same as the sonnet result of 62.34 ohms.

Next the output matching network was designed, with the first step being to plot the required points and transformation on a smith chart.

The smith chart for the output transformation is shown in figure 20.

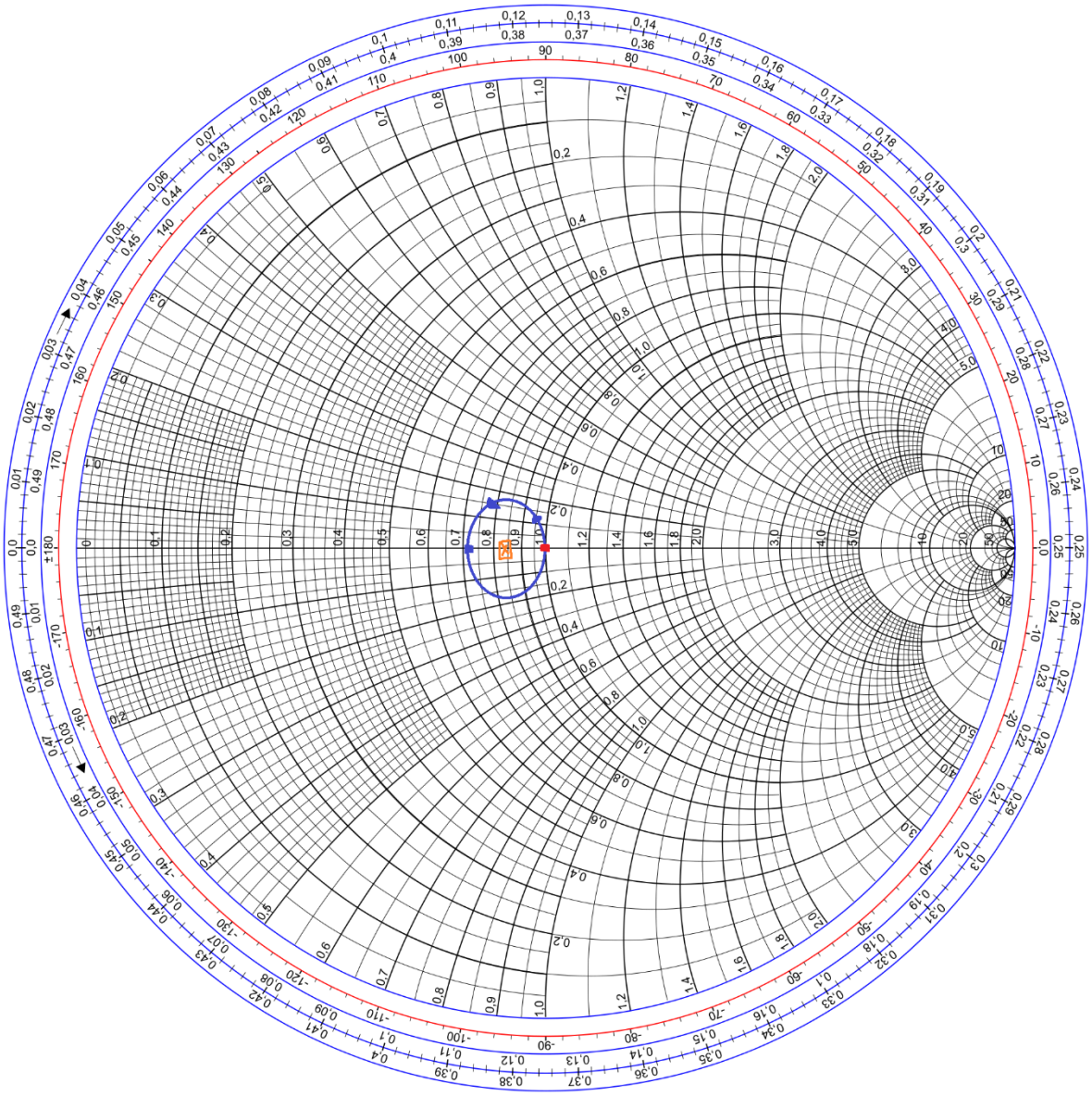

Figure 20. Smith chart with quarter wavelength transformation at load of the system

The smith chart shows that the centre point of the quarter wavelength circle is at an impedance of 42 Ω, and hence a transmission line of characteristic impedance 42 ohms and length λ/4 is required to transform 50 ohms to the required source impedance of 36 Ω.

By using empirical formulae from transmission line theory, the characteristics of this line were calculated. The transmission line characteristics are shown in table 4.

Table 4. Calculated measurements of transformer

Desired Z0(Ω)	Calculated Z0(Ω)	Width(mils)	εeff	Length(mils)
42	41.976	148	3.543	1565

To ensure the calculated measurements for the transmission line were accurate a sonnet model was created to simulate the transformer. The sonnet model of the transmission line is shown in figure 21.

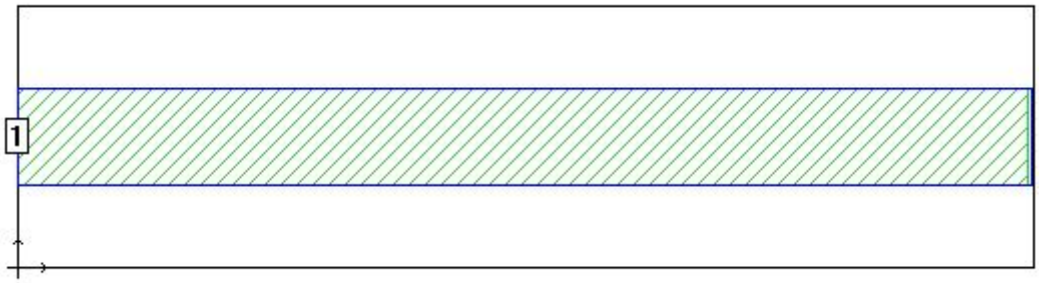

Figure 21. Sonnet model for 42 ohm transmission line

The simulation results of the 42 ohm transmission line are shown in figure 22.

```
Frequency:  1.003 GHZ
  Frequency completed Wed Apr 26 02:15:27 2017.
  De-embedded S-Parameters. 50.0 Ohm Port Terminations.
  Magnitude/Angle. Touchstone Format.
    1.00300000 0.974319 178.68
    !< P1 F=1.003 Eeff=(3.39494417 -0.0704888) Z0=(40.3386771 0.30798457) R=5.75304705 C=0.42495557
```

Figure 22. Sonnet Simulation results for the 42 ohm transmission line

From the simulation it can be seen that the calculated measurements will produce a sufficient characteristic impedance to transform correctly, with the calculated value of 41.976 ohms being roughly the same as the sonnet result of 40.339 ohms.

The complete matching network results are shown in table 5.

Table 5. Complete matching network results

Equation/Sonnet	**Desired Z0(Ω)**	**Calculated Z0(Ω)**	**Width(mils)**	**εeff**	**Length(mils)**
Equation	42	41.976	148	3.543	1565
Sonnet	42	40.339	148	3.4	1565
Equation	64	63.585	72	3.343	1614
Sonnet	64	62.34	72	3.25	1614

With all the dimensions of the matching network confirmed, all parts of the system were now designed and the calculated results could be used to create a manufactured amplifier circuit.

5. PCB Design

To create a PCB of the completed amplifier system design Eagle software was used. This software allowed for a schematic to be created with all the necessary components, as well as a board file that modelled the way the PCB would look after manufacture.

The schematic of the circuit is shown in figure 23.

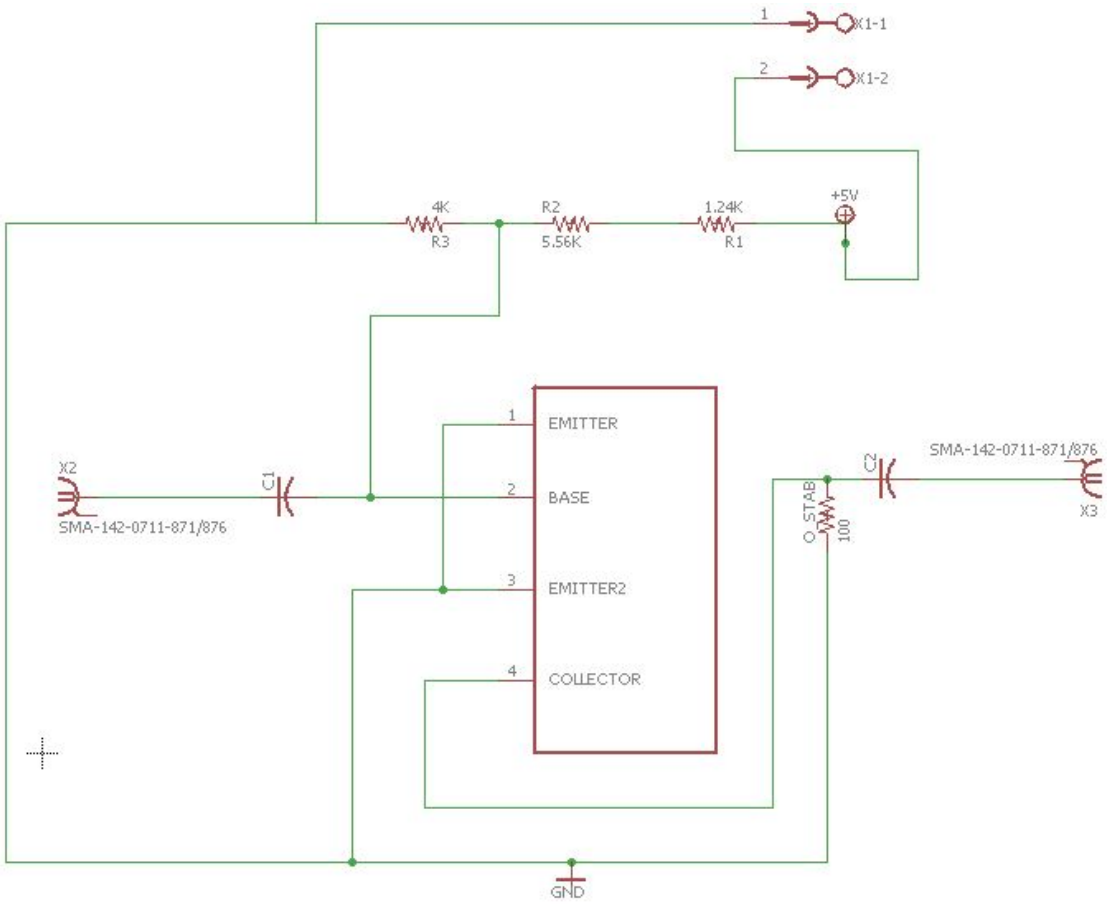

Figure 23. Eagle schematic of amplifier circuit

The schematic displays the connections of the bias circuit resistors, as well as the pins of the BFG403W with regards to the ground and +6 V DC voltage. DC blocking capacitors were added at both the input and output of the circuit to ensure the transistor operated correctly.

On creating a board file of the schematic, the transmission line dimensions from the bias circuit and matching network calculations were used to complete the system.

The board design is shown in figure 24.

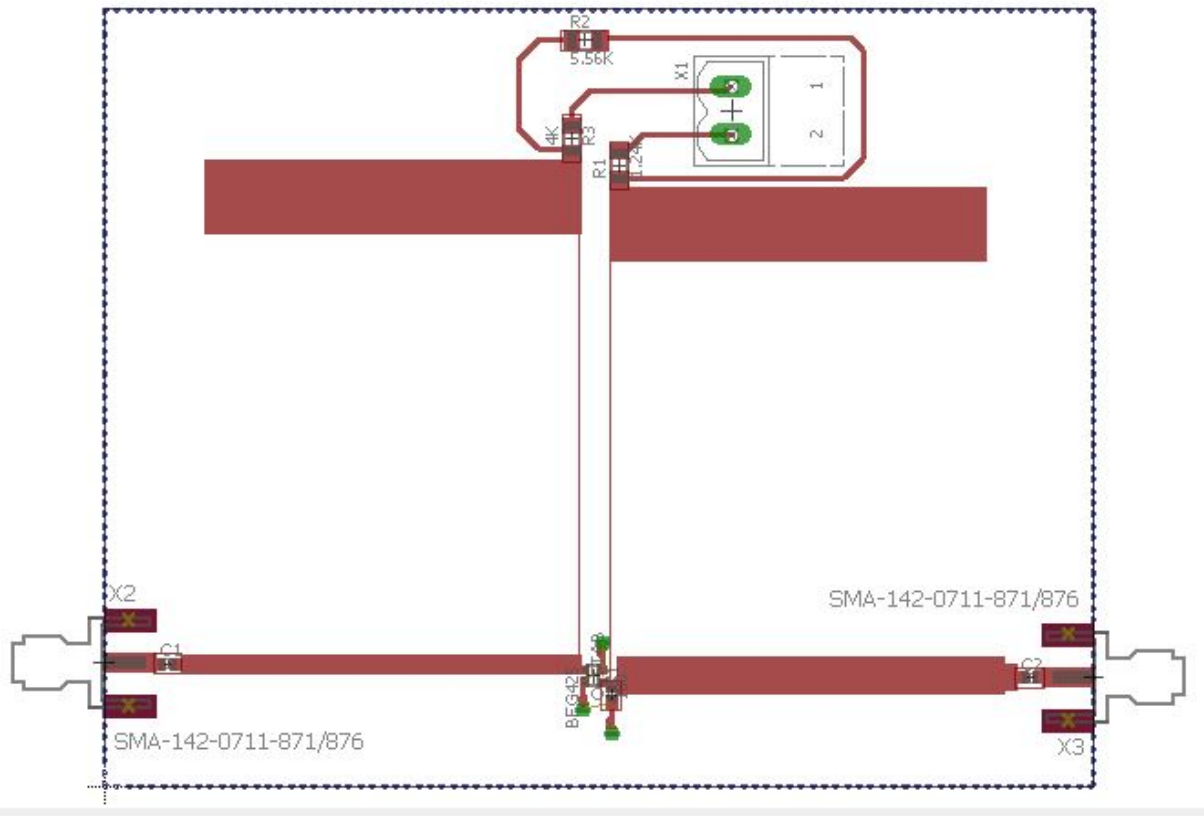

Figure 24. Board design of amplifier circuit

This board design was then used to create the PCB of the amplifier system. The PCB is shown in figure 25.

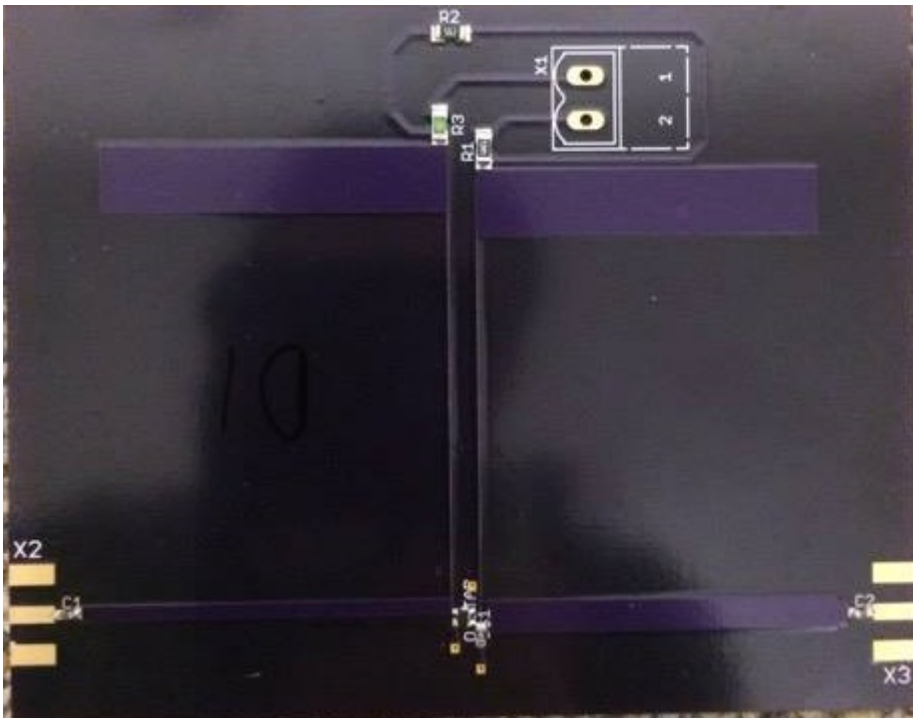

Figure 25. Printed Circuit Board of amplifier system

Testing and Results

With the board manufactured and the components successfully soldered, the amplifier system could be tested using a network analyser. At this stage it was noticed that there was an error in the expected behaviour of the biasing circuit, which was found to be a result of the stability resistor. The decision was made to remove the stability resistor with the aim of sacrificing stability in order to successfully bias the transistor and consequently have an operational amplifier system. To power the system, a DC power supply was connected and set to 5.98 V as shown in figure 26.

Figure 26. Power supply used to power the amplifier circuit

The positive and ground leads from the power supply were connected to the rails of a breadboard, which was subsequently connected to the voltage and ground connection points on the PCB. Measurements were taken for the base voltage and collector voltage before connecting the circuit to the network analyser to ensure power was operating correctly within the circuit. The base voltage was measured to be 0.78 V, and the collector voltage was measured to be 2 V, which were both the desired values for these measurements and therefore the power in the circuit was operating correctly. To protect the analyser from damage, two -20 dB coaxial cables were attached at the input of the amplifier, so as to make the input signal -40 dB. This ensured that the gain applied to the signal from the amplifier would not exceed the level that could damage the equipment.

The amplifier system with coaxial and power connections is shown in figure 27.

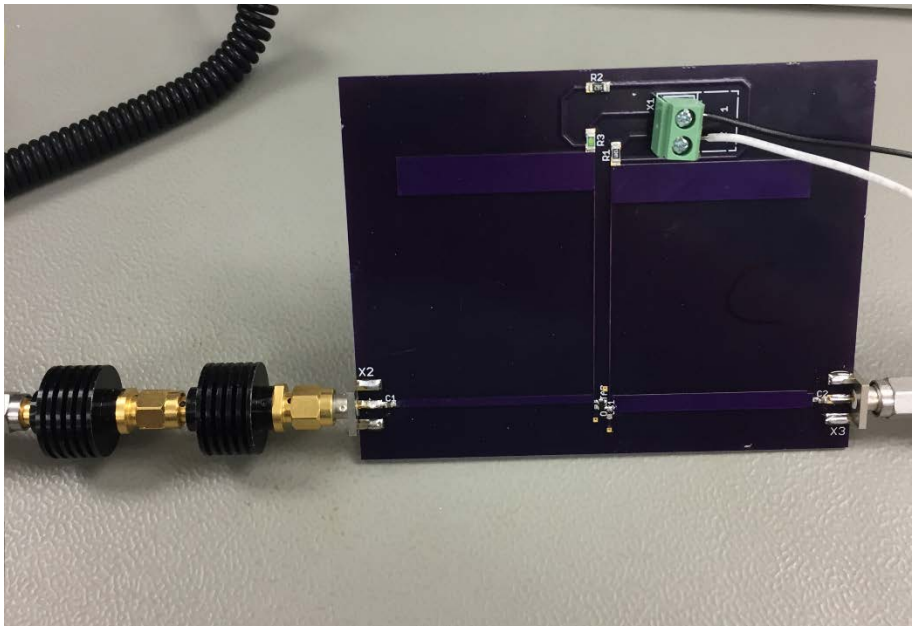

Figure 27. Completed system connected to both DC power and network analyser source

With the connections all in place, analysis was performed over the wideband frequency range, as well as at smaller bandwidths. Measurements were taken for S11, S21, S12, and S22, with a focus on S21 and its phase, group delay, bandwidth and deviation from phase.

The initial analysis of S21 over the wideband range is shown in figure 28.

Figure 28. S21 wideband gain of system

From this graph it can be seen that the output is successfully being amplified, with a value of -27.323 dB at 1 GHz. Since there is -40 dB at the input, the amplifier gain at 1 GHz is found to be 12.677 dB.

To observe the response at a smaller bandwidth, the analyser was adjusted so as to show the 20% bandwidth from 900 MHz to 1.1 GHz. The 20% bandwidth response for S21 is shown in figure 29.

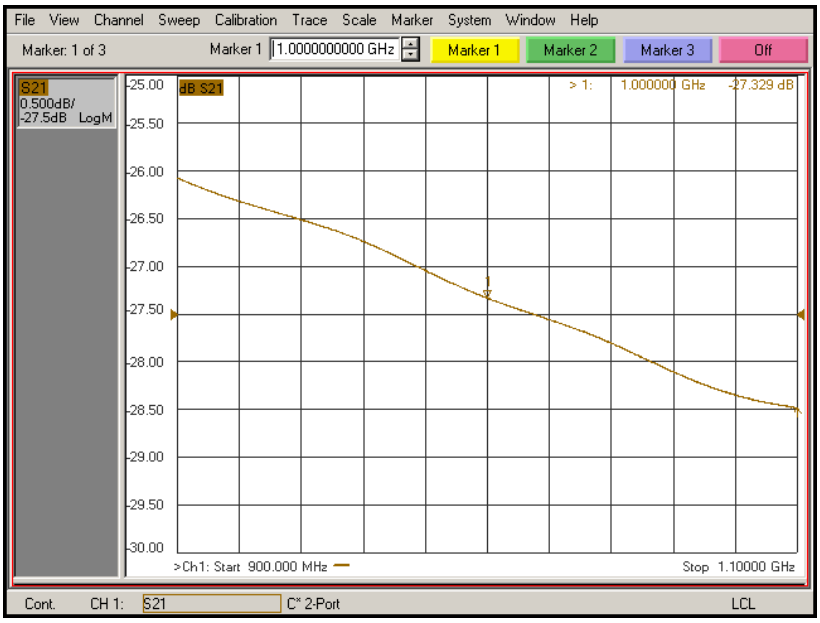

Figure 29. S21 20% bandwidth gain

From this graph it can be seen that over the 20% bandwidth range there is a difference in gain of 2.5 dB.

Finally the 1% bandwidth range was analysed for the gain of S21. The 1% analysis is shown in figure 30.

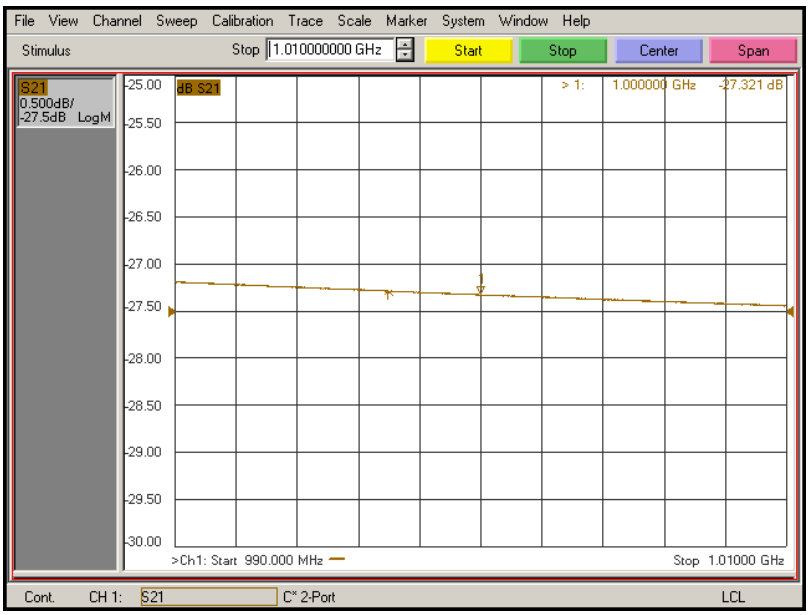

Figure 30. S21 1% bandwidth gain

The 1% bandwidth range has a gain difference of ~0.25 dB.

Next the phase was analysed for S21 at the 20% bandwidth. The phase plot is shown in figure 31.

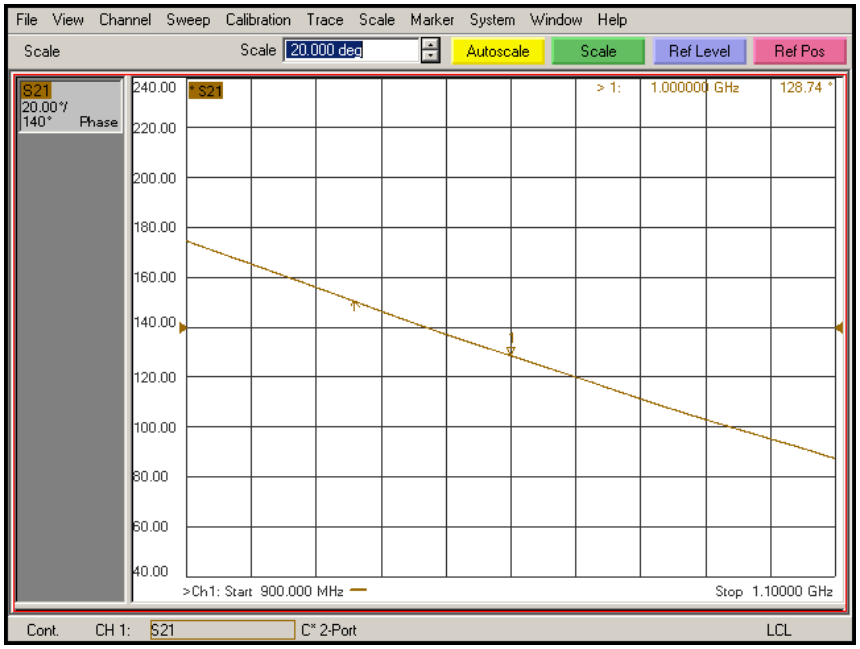

Figure 31. S21 20% bandwidth phase

The phase at 1 GHz was 128.74 degrees, with the desired slope present.

The phase was then analysed for the 10% bandwidth. The 10% phase plot is shown in figure 32.

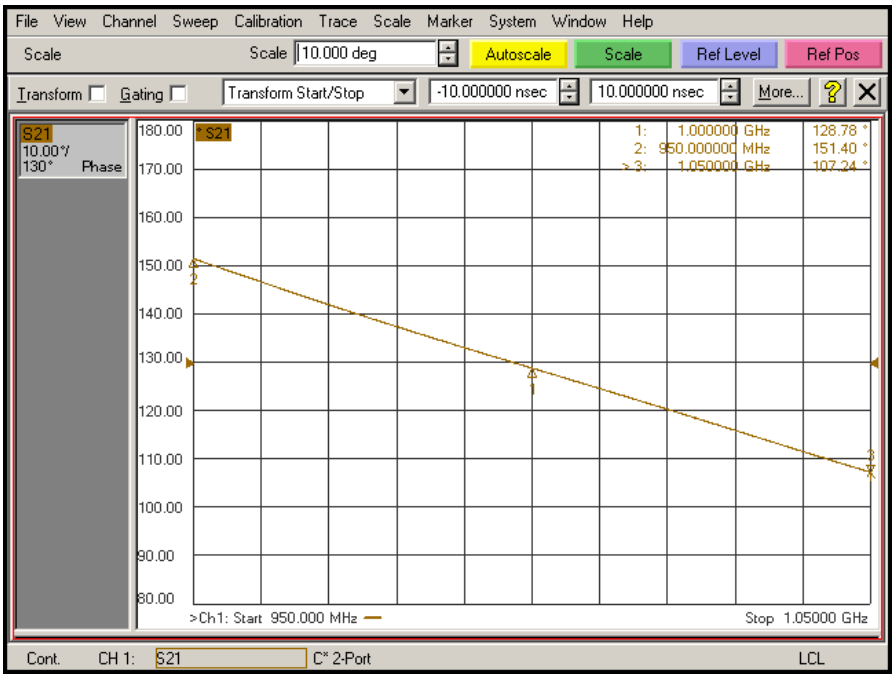

Figure 32. S21 10% bandwidth phase

Across the 10% bandwidth there was a difference in phase of 44.16 degrees.

Next the group delay was analysed for S21. The group delay over the 20% bandwidth is shown in figure 33.

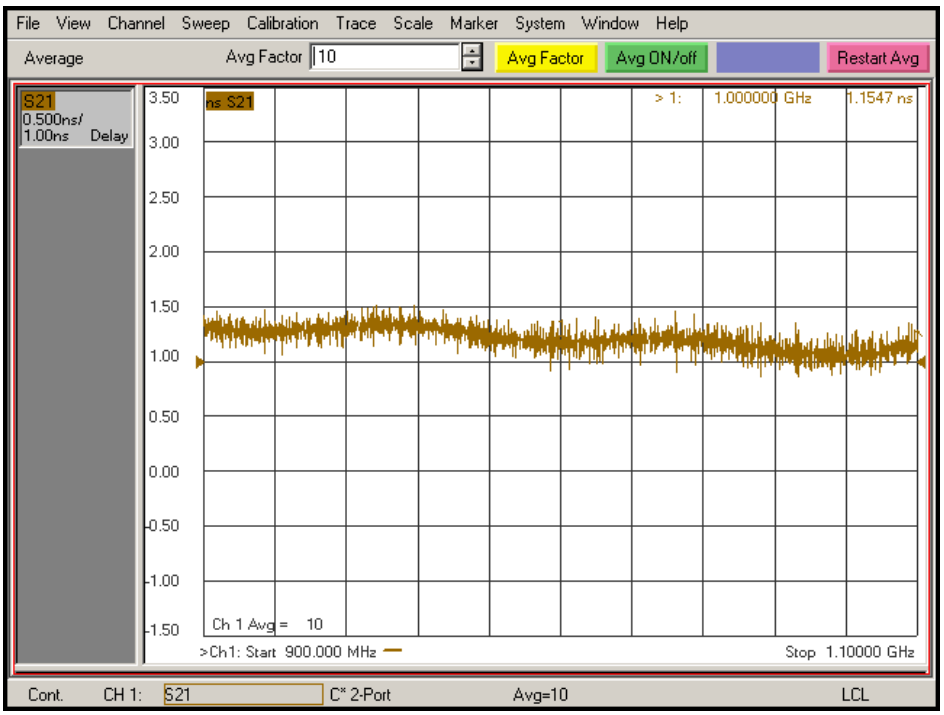

Figure 33. S21 20% bandwidth group delay

The group delay value at 1 GHz was 1.1547 ns.

Finally the deviation of phase was analysed for S21. The deviation of phase for the 20% bandwidth is shown in figure 34.

Figure 34. S21 20% bandwidth deviation of phase

Next the 10% deviation of phase was analysed. The 10% deviation of phase is shown in figure 35.

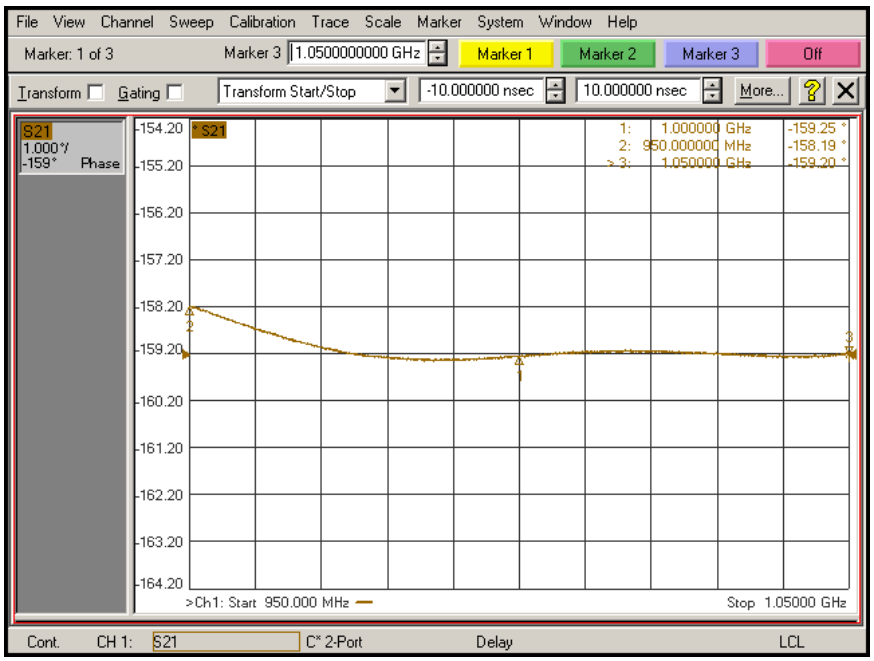

Figure 35. S21 10% bandwidth deviation of phase

From this graph it can be seen that the 10% bandwidth has a deviation of linear phase of about 1 degree. Finally the 1% bandwidth deviation of phase was observed. The 1% deviation of phase is shown in figure 36.

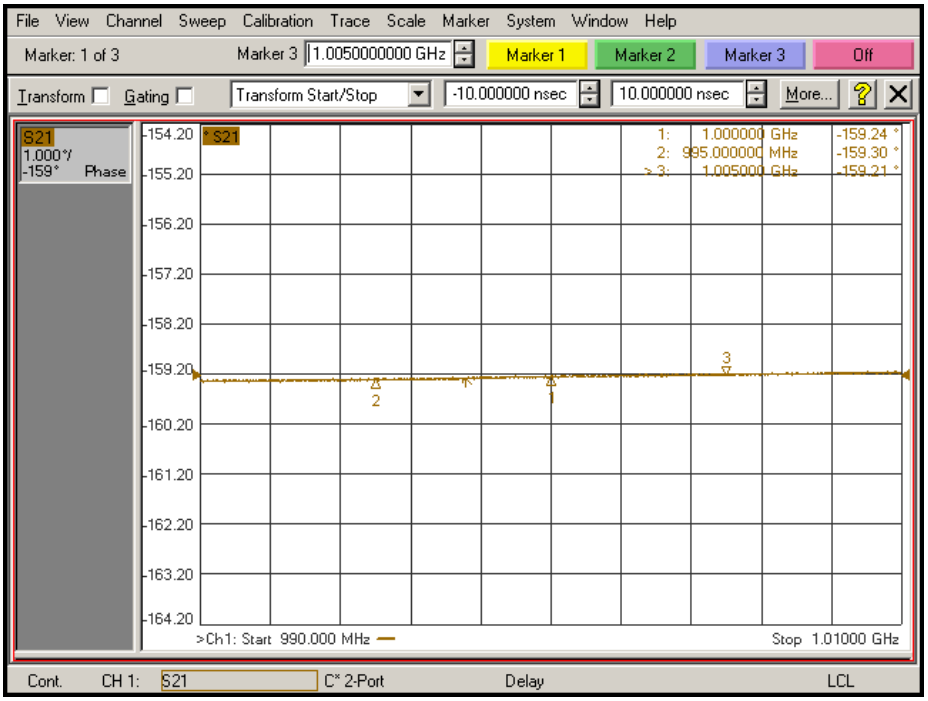

Figure 36. S21 1% bandwidth deviation of phase

From this graph it can be seen that over the 1% bandwidth there is a deviation of phase of less than 0.1 degrees.

Next the analyser was used to observe the response of S11. The wideband gain of S11 is shown in figure 37.

Figure 37. S11 wideband gain

This response was also observed on a smith chart. The smith chart for S11 is shown in figure 38.

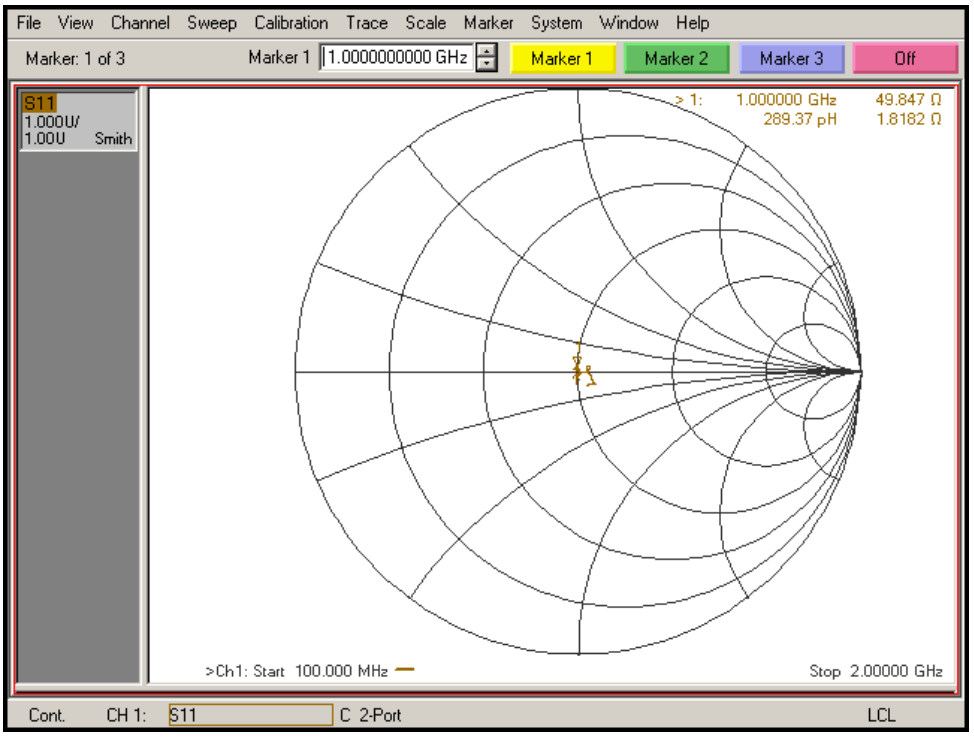

Figure 38. S11 Smith chart gain

The smith chart shows the response successfully circling around the centre 50 Ω point.

The analyser was then used to observe the response of S22. The gain of S22 is shown in figure 39.

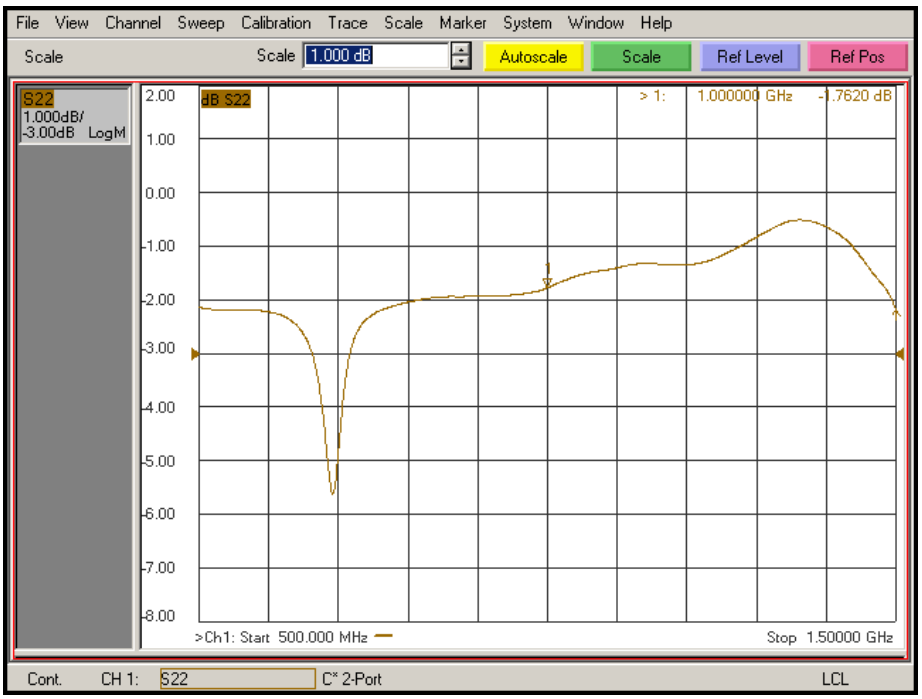

Figure 39. S22 wideband gain

This response was also observed on a smith chart. The smith chart for S22 is shown in figure 40.

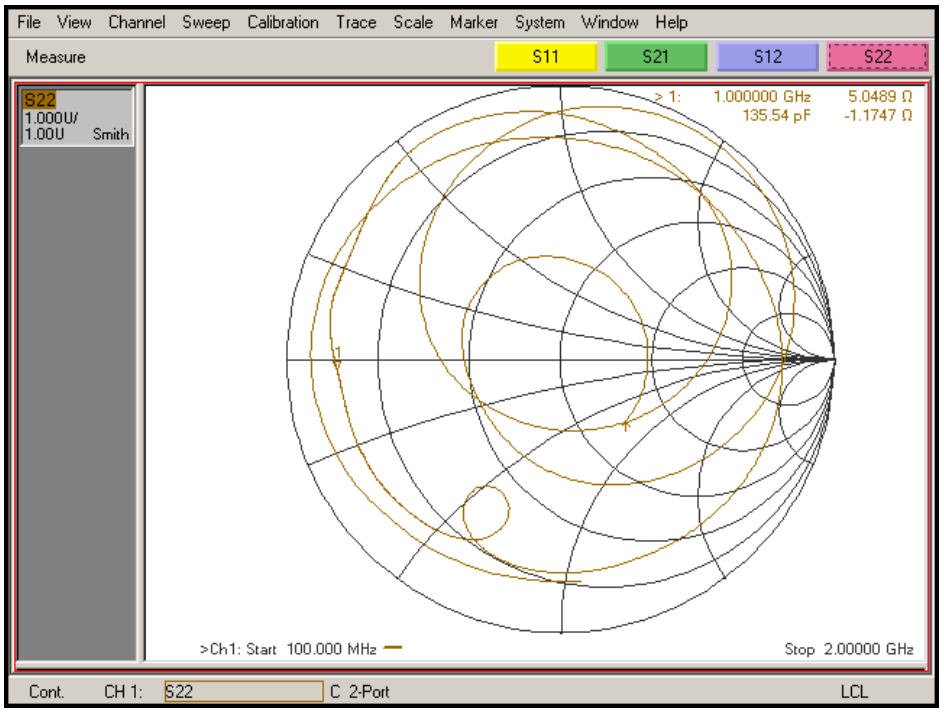

Figure 40. S22 Smith chart gain

The final response analysed was S12. The gain of S12 is shown in figure 41.

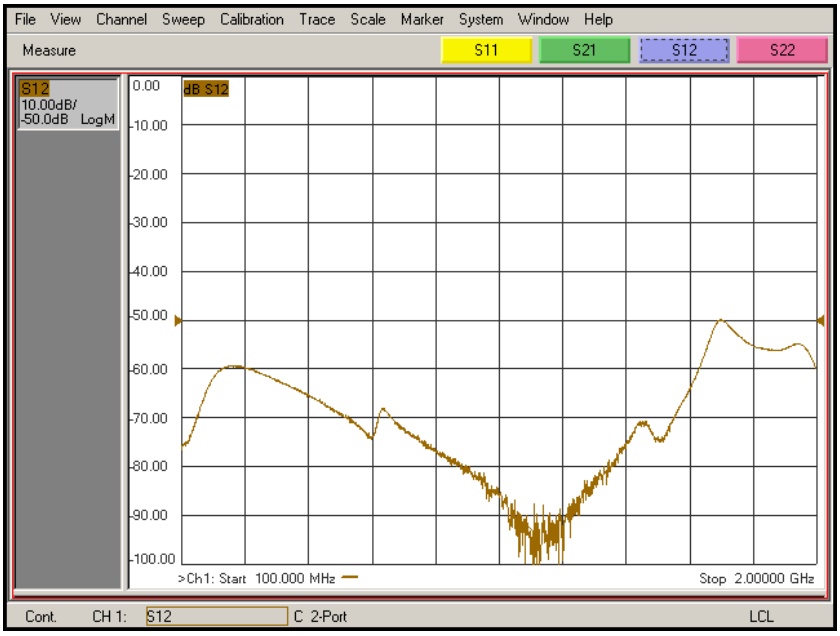

Figure 41. S12 wideband gain

By observing all the data, the amplifier system operates correctly and produces positive results. With the unilateral design and gain circle methods utilised, it was calculated that the maximum gain possible from the amplifier system would be 13.56 dB. The measured gain value of 12.677 dB was therefore a positive result, especially with the necessary removal of the stability resistor. The phase and deviation of phase results over the 10% bandwidth were both satisfactory also, with the amplifier showing strong efficiency characteristics.

The one negative aspect of the final system design was the error with the stability resistor. On re-design, this resistor would be required to come after the DC blocking capacitor so as to prevent interference with the biasing circuit. The removal of this resistor from the PCB did not prevent the amplifier from operating successfully, however the removal of this stability component created an undesired S22 gain of ~2 dB. On comparing the S-parameters of the transistor and of the system with the stability resistor, the Matlab simulations in figure 42 show that the removal of the resistor does in fact create an undesired increase in S22. A re-design would hence factor in these results to improve system performance and stability.

```
s22 =

   0.8870 - 0.3300i

>> abs(s22)

ans =

    0.9464
```

```
s22 =

   0.2907 - 0.1519i

>> abs(s22)

ans =

    0.3279
```

Figure 42. Matlab simulation of S22 without the resistor (left), and with the resistor (right)

Despite this, the overall performance of the amplifier was satisfactory and successfully applied gain to a 1 GHz input signal. The final performance parameters of the amplifier are shown in table 6.

Table 6. Final Amplifier performance parameters

Gain at Centre Frequency	**20% BW**	**10% BW**	**1% BW**
12.7 dB	±1.25 dB	±0.7 dB	±0.1 dB

Conclusion

In conclusion, this project was successful at delivering an operational RF amplifier system. A greater understanding of the key features of an RF amplifier system was developed through research into the different design techniques available, before applying these techniques throughout the design process. By using the simulation software tools Multisim, Matlab and Sonnet it was possible to assess the accuracy of each step of the design process before proceeding to manufacture.

Through the implementation of basic circuit theory, transmission line theory and the amplifier design tools, a fully operational RF amplifier system was designed and manufactured. The amplifier succeeded in meeting the target gain value of >10 dB with a final gain of 12.7 dB at 1 GHz.

Further improvements to the project system could be made with regards to the stability resistor, as well as research into developing a system that targets a higher level of output gain by utilising the bilateral design method.

References

Joseph F White. (2004). Transistor Amplifier Design. In: White *High Frequency Techniques*. New Jersey: John Wiley & Sons. p399-473.

Reinhold Ludwig & Gene Bogdanov. (2009). RF Transistor Amplifier Design. In: Pearson *RF Circuit Design*. USA: Pearson. p485-557.